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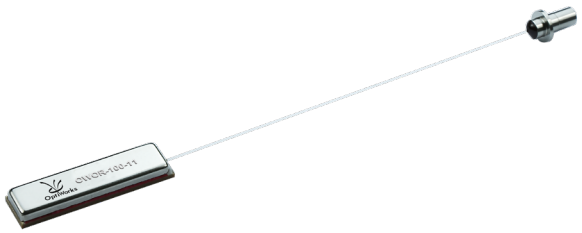
Transceiver 100G CWDM4 (ROSA 2km spec) OWOR-100-11



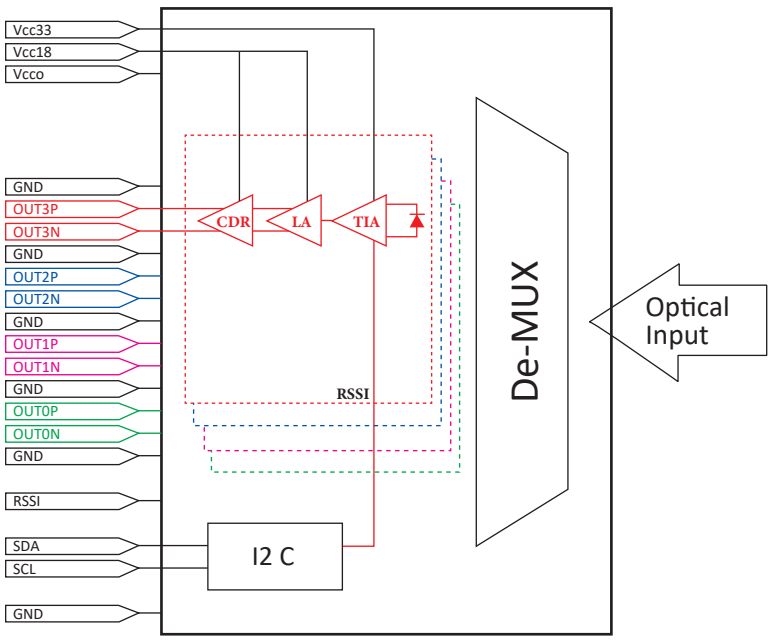
Key Features

- Up to 25.78125 ±100 ppm Operation (NRZ)
- PIN Photodiode (PIN-PD) Base Quad ROSA for CWDM4
- Integrated TIA/LA/CDR
- Programmable Output Swing, Squelch and De-Emphasis
- 2 Wire Communication (Up to 400 kHz)
- CWDM4 Optical De-MUX Integrated
- Pigtail with LC Connector
- SMT Style for Electrical RF Signals

Applications

- CWDM4 MSA
- QSFP28/CFP2/CFP4 Transceiver Modules
- On Board Optics

Modular Block Diagram



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Optical and Electrical Characteristics

T_C = 0°C to 80°C, (unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.
Bit Rate		NRZ, each lane		25.781 Gb/s	
Operational Case Temperature	T_C		0℃	25℃	80℃
PD					
Peak Wavelength for L0	L_0[1]	for L0	1264.5 nm	1271 nm	1277.5 nm
	L_1[1]	for L1	1284.5 nm	1291 nm	1297.5 nm
	L_2[1]	for L2	1304.5 nm	1311 nm	1317.5 nm
	L_3[1]	for L3	1324.5 nm	1331 nm	1337.5 nm
PD Responsivity	R	CW	TBD	TBD	TBD
Damage threshold, each lane [2]	Pd	CW	3.5 dBm		
Maximum Overload, each lane [1]	Pmax	OMA	2.5 dBm		
Minimum Sensitivity, each lane [1, 3]	Pmin	OMA		-10 dBm	
SRS eye mask definition (X1, X2, X3, Y1, Y2, Y3)[1, 4, 5]		4th Bessel		Refer to Figure1 (0.39, 0.5, 0.5, 0.39, 0.39, 0.4)	
Optical Return Loss	ORL	λ = 1300 nm			26 dB
TIA/LA/CDR					
Core Power Supply Voltage (1.8 V)	Vcc18,Vcco		1.71 V	1.80 V	1.89 V
TIA Power Supply Voltage (3.3 V)	Vcc33		2.97 V	3.3 V	3.47 V
Differential Output Impedance Termination	R_{TERM}			100 ohm	
Differential Output Amplitude [8]	$R_{X\,X}$	AC	300 mVppd	800 mVppd	930 mVppd
Rx x Rise/Fall Time [12]	T_{RISE}/T_{FALL}	20~80%		16 psec	20 psec
Output Differential Return Loss [6]	S22				TBD
RSSI Range	$RSSI_{Range}$		4 µA		504 µA
Program Output De-emphasis [8, 12]	DE		0 dB		7.5 dB
Total Output Jitter [10]	t_{JIT}				TBD
Loss Of Signal [7, 8]	LOS				TBD
LOS Hysteresis [7, 8]	LOS_{HYST}		1.5 dB		2.5 dB
LOS Assert Time [9]	Tast				100 µsec
LOS De-assert Time [9]	Tdeast				100 µsec
CDR Lock Time	T_{LOCK}			0.7 msec	2 msec
LOL Timing from occurrence to triggering [11]	T_{LOCK}				0.5 msec

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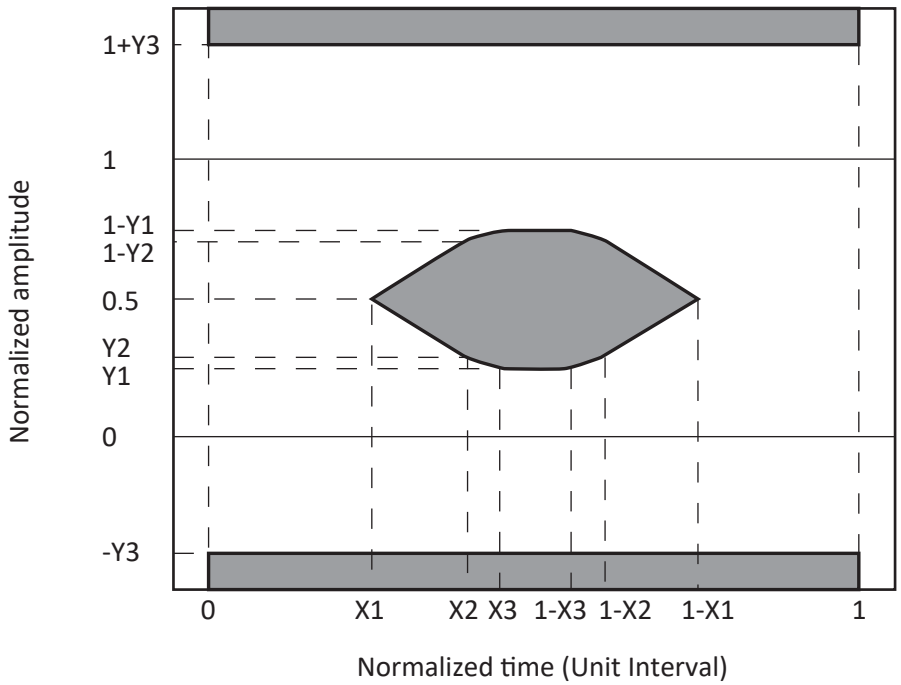
Parameter	Symbol	Condition	Min.	Typ.	Max.
I2C					
CMOS Output Logic High	V_{OH_CMOS}	I_{OH} = 4 mA	1.5 V	1.7 V	1.92 V
CMOS Output Logic Low	V_{OL_CMOS}	I_{OH} = 4 mA		0 V	0.3 V
Open Drain Output Logic High	V_{OH_OD}	I_{OH} = 4 mA	0.8xVcc-EXT		Vcc-EXT
Open Drain Output Logic Low	V_{OL_OD}	I_{OH} = 4 mA		0 V	0.3 V
Input Logic High	V_{IH}		0.75xVcc18		3.465 V
Input Logic Low	V_{IL}		0 V		0.2xVcc18
Total Power Dissipation	Ptotal			0.71 W	TBD

1: 25.8Gbps, PRBS=2^{31}-1.
2: The receiver shall be able to tolerate, without damage, continuous exposure to an optical signal having this average power level.
3: BER=5E-5 and normative specification.
4: BER=5E-5, Vertical eye closure penalty = 1.9 dB, J2 Jitter = 0.33 UI and J4 Jitter = 0.48 UI.
5: See mark in Figure1.
6: Measured using MACOM EVM and an output latched high or low.
7: The LOS assert/de-assert levels are independent of CDR enable or CDR bypass modes.
8: Typical programmable range.
9: Minimum of 6 dB change in optical signal.
10: CDR enabled.
11: The time it takes to assert the LOL from valid input data to invalid input data. The valid input data is data within range covered by the data rates.
12: Measured with 100 Ω differential load.

Figure 1. SRS Eye Mask



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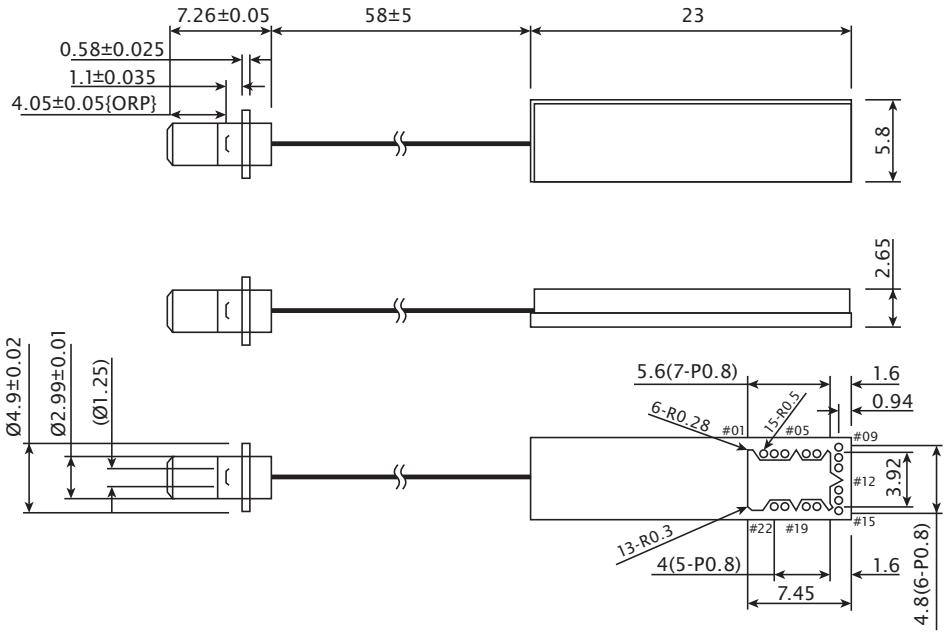
Absolute Maximum Ratings

T_C = 25°C, (unless otherwise specified)

Parameter	Symbol	Condition	Min.	Max.
Maximum Optical Input Power	PIN	Each lane, CW	4 dBm	
Core Power Supply Voltage (1.8V)	Vcc18, Vcco		-0.5 V	2 V
TIA Power Supply Voltage (3.3V)	Vcc33		-0.5 V	4 V
DC Input Voltage (CMOS)	VIN CMOS	SCL	GND-0.5 V	3.8 V
Maximum Current from RSSI	IRSSI		4 mA	
Maximum Current from OUTP/N	Iout		20 mA	
Storage Temperature	Tstg		-40 degC	85 degC
Electrical Discharge Voltage(HBM)	VESD, HBM			TBD

Dimensions



Unit: mm

Pin Configuration

Pin#	Symbol	Description
1,5,8,9,12,15,16,19,22	GND	Ground
2	Vcc33	+3.3 V power supply
3	NC	No Connect
4	Vcco	+1.8 V power supply
6	OUT3P	positive data output for L0
7	OUT3N	negative data output for L0
10	OUT2P	positive data output for L1

Pin#	Symbol	Description
11	OUT2N	negative data output for L1
13	OUT1P	positive data output for L2
14	OUT1N	negative data output for L2
17	OUT0P	positive data output for L3
18	OUT0N	negative data output for L3
20	SCL	two-wire serial interface clock
21	SDA	two-wire serial interface data

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